

UCD30xx General Purpose 12-bit ADC (ADC12) Programmer's Manual

Table of Contents

1. Module Overview	3
2. Operational description.....	5
2.1 Conversion.....	5
Sequencer	5
ADC Sequence Select Register 1 (ADCSEQSEL1).....	5
ADC Sequence Select Register 5 (ADCSEQSEL5).....	5
ADC Sequence Select Register 6 (ADCSEQSEL6).....	6
ADC Control Register 1 (ADCCTRL1).....	7
Channel Mapping	9
PMBUS Address Detection.....	10
The current sources are disconnected as default to let application use Ch-0 and Ch-1 for purposes other than PMBus detection. Therefore the bits IBIAS_A_ENA and IBIAS_B_ENA in PMBus Trim Register (PMBTRIM) needs to be set for proper PMBus address detection.....	10
PMBus Trim Register (PMBTRIM).....	10
Digital Comparators	11
ADC Digital Compare Results Register (ADCCOMPRESULT)	11
Useful C statements:	13
ADC Registers	14
ADC Control Register 1 (ADCCTRL1).....	14
ADC Test Control Register (ADCTSTCTRL)	15
ADC Sequence Select Register 1 (ADCSEQSEL1).....	15
ADC Sequence Select Register 2 (ADCSEQSEL2).....	15
ADC Sequence Select Register 3 (ADCSEQSEL3).....	16
ADC Sequence Select Register 4 (ADCSEQSEL4).....	16
ADC Sequence Select Register 5 (ADCSEQSEL5).....	17
ADC Sequence Select Register 6 (ADCSEQSEL6).....	17
ADC Result Registers 0-15 (ADCRESULTx, x=0:15).....	18
ADC Digital Compare Limits Register 0-5 (ADCCOMPLIMx, x=0:5)	19
ADC Digital Compare Enable Register (ADCCOMPENA).....	19
ADC Digital Compare Results Register (ADCCOMPRESULT)	20

1. Module Overview

The 12 bit 200 KSPS general purpose ADC in UCD30xx is referred to as ADC-12.

The ADC-12 module contains the wrapper and conversion logic for auto sequencing a series of ADC conversions. Each sequence has the choice of selecting any one of the 16 input channels (16 channels/15 external pins in the 80 pin version, 12 channels/11 pins in 64-pin and 10 channels/9 pins in 48-pin) available through an analog multiplexer to the ADC. The ADC-12 also has a total of 16 extra internal channels for test purposes.

Once converted, the selected channel value is stored in the appropriate result register. Input channels can be sampled in any desired order or programmed to repeat the same channel multiple times during a conversion sequence. Selected channel conversions are also stored in the result registers in time order, where result 0 is the first conversion of a session and result 15 is the last. The maximum number of conversions (MAX_CONV: bits 4:7 in ADCCTRL1) in an auto-sequenced session that can be programmed is 16.

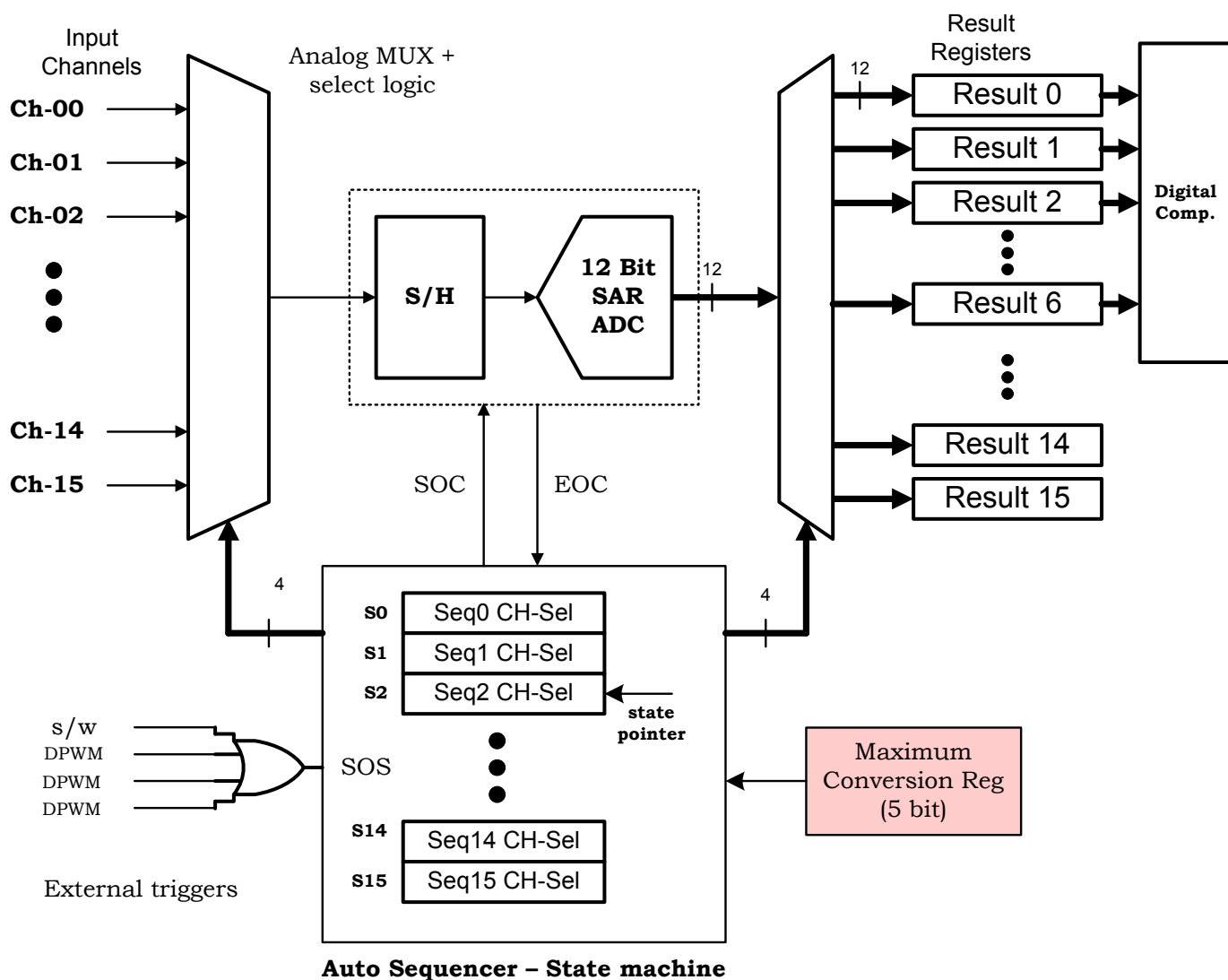


Figure 1.1: ADC wrapper top level view with Auto sequencer

2. Operational description

2.1 Conversion

The ADC Conversion is controlled by a state machine that generates the necessary control signals for the Successive Approximation Register (SAR) ADC operation. The binary search algorithm, sampling time and bit timing are controlled by the logic for converging on the input analog signal and generating the 12 bit result.

Sequencer

The measurement sequencer is capable of “auto-sequencing” up to 16 conversions of any channel in a single sequencing session. The result of each conversion is stored in a 16 word result buffer. The desired input channel for each sequenced conversion is programmed in the Channel Select Sequence registers. So, each Channel Select Sequence register can be programmed with any of the 16 analog channel inputs to the ADC. The sequence always starts with the programmed channel input in the first Channel Select Sequence register and progresses to the next Channel Select Sequence register until the maximum count register value is reached. The maximum count register defines the number of conversions in the sequence. Each of the 4 bit channel selection fields can be programmed with any channel. Also, the same channel may be selected multiple times.

The default per channel sequence time is 5 μ S. Sequence time consists of 2 μ S of sampling time plus 3 μ S of conversion time. Therefore the total throughput of the ADC is 200 KSPS.

ADC Sequence Select Register 1 (ADCSEQSEL1)

Address FFF7DC08

Bit Number	14:10	9:5	4:0
Bit Name	SEQ2	SEQ1	SEQ0
Access	R/W	R/W	R/W
Default	00000	00000	00000

.....

ADC Sequence Select Register 5 (ADCSEQSEL5)

Address FFF7DC18

Bit Number	14:10	9:5	4:0
Bit Name	SEQ14	SEQ13	SEQ12
Access	R/W	R/W	R/W
Default	00000	00000	00000

ADC Sequence Select Register 6 (ADCSEQSEL6)

Address FFF7DC1C

Bit Number	4:0
Bit Name	SEQ15
Access	R/W
Default	00000

A total of 6 sequence selection registers.
The bits b4, b9, b14 to b31 are reserved and should always be set to zero.

The following are few C-language statements to demonstrate software examples that may be used to interact with ADC interface and specific registers.

This will also help the programmer to get better orientated inside the “ready made structures” provided by the supplied header files. Using the following examples and code composer studio, the user should be able to locate the relevant registers as needed.

Useful C statements:

```
AdcRegs.ADCSEQSEL1.bit.SEQ0 = 15;
```

```
//Means that channel 15 (the very last input channel) is selected as the very first measurement in the  
//measurement sequence.
```

```
AdcRegs.ADCSEQSEL2.half.HALF0 = 5 + (6 << 5) + (7 << 10);
```

```
//Means, the channels 5, 6 and 7 are set to be the fourth, fifth and the sixth (SEQ3 to SEQ5) respectively  
//in the measurement sequence.
```

The sequencer can be triggered by the CPU or by external trigger sources. The external trigger sources are the DPWM module A and B outputs. Additionally, the sequence can be set up to perform one single sweep sequence or continually start the sequence on the external trigger source. The sequencer can be enabled to generate a CPU interrupt at the end of the sequence.

ADC control register (ADCCTRL) also provides an end of measurement indication bit. This Indication bit is cleared on read to ensure valid complete status.

ADC Control Register 1 (ADCCTRL1)

Address FFF7DC00

Bit Number	22	21	20:16	15:13
Bit Name	COMP_INT_FLG	INT_FLG	CURRENT_CH	RESERVED
Access	R	R	R	-
Default	-	-	-	000

Bit Number	12	11	10	9
Bit Name	COMP_INT_ENA	INT_ENA	EXT_TRIG_ENA	SW_START
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	8	7:4	3:1	0
Bit Name	SINGLE_SWEEP	MAX_CONV	EXT_TRIG_SEL	ADC_ENA
Access	R/W	R/W	R/W	R/W
Default	0	0000	000	0

Useful C statements:

```
#define ADCCTRL1_HALF0_SINGLE_SWEEP    0x100
#define ADCCTRL1_HALF0_MAXCONV_SHIFT   4
#define ADCCTRL1_HALF0_ADC_ENA         1
```

```
AdcRegs.ADCCTRL1.half.HALF0 = ADCCTRL1_HALF0_SINGLE_SWEEP +
(7 << ADCCTRL1_HALF0_MAXCONV_SHIFT) + ADCCTRL1_HALF0_ADC_ENA;
```

//Means; enable ADC, set up for 16 samples, single sweep, and software trigger, no interrupts.

```
AdcRegs.ADCCTRL1.bit.SW_START = 1;
```

//Means; the ADC is instructed to start a new conversion sequence.

Please note, the end of sequence should not be determined by polling the Latched Sequence Complete Indication bit.

Since this bit may occasionally get cleared if it gets set too late during the read, asynchronous polling of this indication bit may be unreliable.

Below are two reliable alternatives to determine the end of a conversion sequence.

First alternative:

- 1) Enable interrupts both at the local (ADC) and CPU (Central Interrupt Module) levels.
- 2) Utilize the ADC's end of sequence CPU interrupt, and read the results inside the related interrupt routine.

Second alternative:

- 1) Run the ADC in single sweep mode.
- 2) Enable the interrupt only at the local (ADC) level.
- 3) Before the attempt to read the results, determine the end of measurement sequence by polling the relevant bit in the pending interrupt read location register (INTREQ) in the Central Interrupt Module (CIM).

C code examples:

```
AdcRegs.ADCCTRL1.bit.INT_ENA = 1; // Means: enable interrupt at local ADC level
```


CimRegs.REQMASK.bit.REQMASK25 =1; // Means: Enable ADC interrupt at CPU level.

if(CimRegs.INTREQ.bit.INTREQ25 == 1) // Means; if ADC measurement completed.

Temporary1 = AdcRegs.ADCCTRL1.half.HALF1; // Means :read and clear completion flags

Temporary2 = AdcRegs.ADCRESULT3.all; // Read the fourth result register

Channel Mapping

Channel #	Internal / External signals	Availability in 80-pin version	Availability in 64-pin version	Availability in 48-pin version	Description
Ch-15	Temp Sensor	Yes	Yes	Yes	Internal Temperature Sensor
Ch-14	AD-14	Yes	No	No	GP Analog input to ADC12
Ch-13	AD-13	Yes	No	No	GP Analog input to ADC12
Ch-12	AD-12	Yes	No	No	GP Analog input to ADC12
Ch-11	AD-11	Yes	No	No	GP Analog input to ADC12
Ch-10	AD-10	Yes	Yes	No	GP Analog input to ADC12
Ch-9	AD-09	Yes	Yes	No	GP Analog input to ADC12
Ch-8	AD-08	Yes	Yes	Yes	GP Analog input to ADC12
Ch-7	AD-07	Yes	Yes	Yes	GP Analog input to ADC12
Ch-6	AD-06	Yes	Yes	Yes	GP Analog input to ADC12
Ch-5	AD-05	Yes	Yes	Yes	GP Analog input to ADC12
Ch-4	AD-04	Yes	Yes	Yes	GP Analog input to ADC12
Ch-3	AD-03	Yes	Yes	Yes	GP Analog input to ADC12
Ch-2	AD-02	Yes	Yes	Yes	GP Analog input to ADC12
Ch-1	AD-01	Yes	Yes	Yes	PMBus Addr ID #2 or GP Analog input
Ch-0	AD-00	Yes	Yes	Yes	PMBus Addr ID #1 or GP Analog input

Table 2.1 – Analog input mapping to ADC12 (Non-Test Mode)

PMBUS Address Detection

The PMBus needs six address bits to uniquely identify devices on the bus, where two physical ADC pins have been assigned to decode the address. Thus each pin is capable of resolving one of eight possible states for decoding three bits. For address detection, the 10uA current sources need to be enabled in the PMBUS trim register for driving current out of channels 0 and 1. Where resistors are connected to ground for producing a voltage in the range from 0.25V to 2.00V, resulting in .25 volts per address bit step. Grounded inputs or open pins would then result in non-valid states. Then an ADC conversion can be performed on those channels for detecting the address. The resistor values shown in the table are 1% EIA standard values.

The current sources are disconnected as default to let application use Ch-0 and Ch-1 for purposes other than PMBus detection. Therefore the bits IBIAS_A_ENA and IBIAS_B_ENA in PMBus Trim Register (PMBTRIM) needs to be set for proper PMBus address detection.

PMBus Trim Register (PMBTRIM)

Address FFF7F624

Bit Number	4	3	2:0
Bit Name	IBIAS_B_ENA	IBIAS_A_ENA	IBIAS_TRIM
Access	R/W	R/W	R/W
Default	0	0	000

Resistor Value	Pin Voltage	Addr Value
open	Vdd	Invalid
200k	2.00V	111
174k	1.74V	110
150k	1.50V	101
124k	1.24V	100
100k	1.00V	011
75k0	0.75V	010
49k9	0.50V	001
24k9	0.25V	000
Ground	0.00V	Invalid

Digital Comparators

The ADC wrapper logic has digital comparators that can be used to compare the result registers against programmed high and low limits. The first 6 conversion result registers (Result 0 – Result 5) of the ADC sequence are the ADC results having digital comparator functionality. Therefore, for any signals requiring auto limit monitoring, the user must use these 6 ADC conversion slots for monitoring of those signals. All 12 bits of conversion result are used for comparison. The Digital Comparator logic provides 12 status bits for monitoring, two from each ADC Result comparison. These status bits indicate whether the ADC Result is higher or equal to the Limit High register setting, or it is lower or equal to the Limit Low register setting.

ADC Digital Compare Results Register (ADCCOMPRESULT)

Address FFF7DC7C

Bit Number	11:10	9:8	7:6
Bit Name	RESULT5	RESULT4	RESULT3
Access	R	R	R
Default	-	-	-

Bit Number	5:4	3:2	1:0
Bit Name	RESULT2	RESULT1	RESULT0
Access	R	R	R
Default	-	-	-

Two bit are indicating the status of each comparator output the most significant bit between the two will indicate if the upper limit is exceeded and the lease significant bit indicates if the lower limit is exceeded. For example: Bits 11-10: RESULT5 – Digital Comparator 5 Result

Bit 11: Upper Limit Indication

0 = Limit not exceeded

1 = Limit exceeded

Bit 10: Lower Limit Indication

0 = Limit not exceeded

1 = Limit exceeded

Please note: Polling of digital comparator result register will not provide a good indication of comparator's status. This register needs to read only at the time the digital comparator interrupt is serviced. The relevant interrupt will only be invoked if ADC-12 output value moves from the inside the limits area to the outside the limits area and exceeds either the low or the high limit.

No interrupt is invoked if ADC-12 output value moves from the outside the limits area back to the area within the limits.

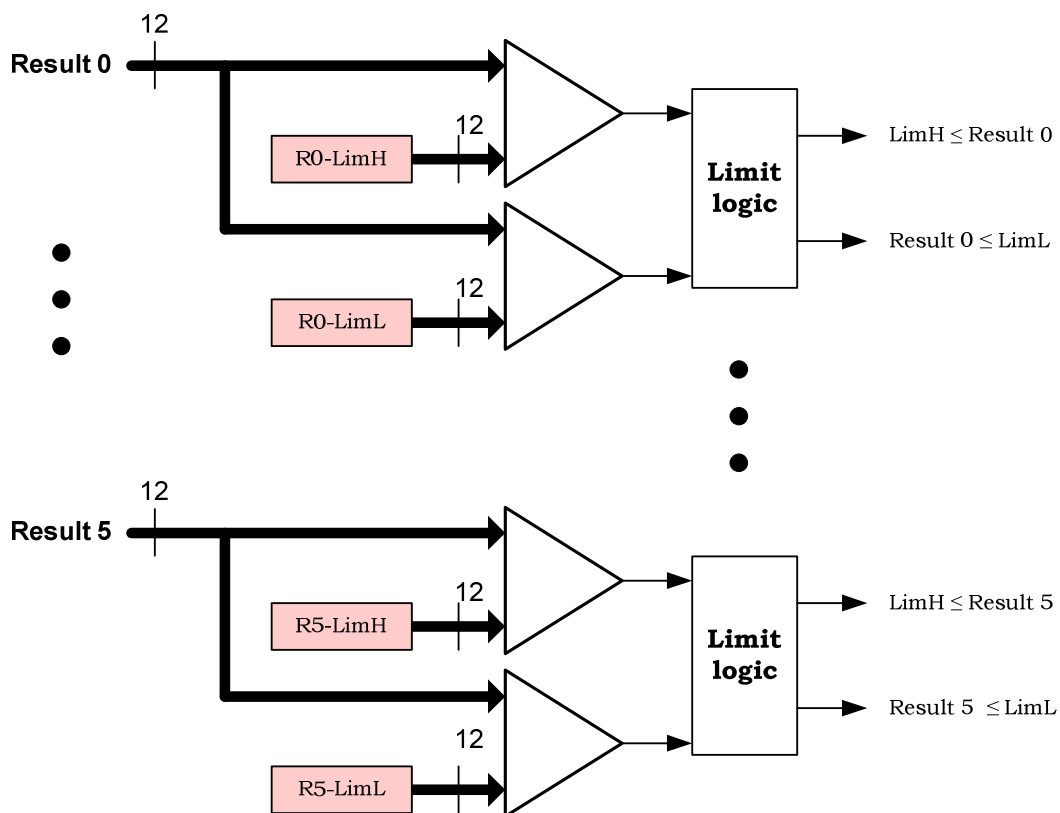


Fig 3.1 – Digital Comparators

Useful C statements:

```
if (AdcRegs.ADCCOMPRESULT.bit.RESULT0 == 1)
//Means: if the lower limit is exceeded on the first comparator
```

```
If (AdcRegs.ADCCOMPRESULT.bit.RESULT5 == 2) // Upper bit among the two bits is set
// Means: if Upper-Limit on sixth comparator is exceeded, Upper-bit <-> Upper-Limit
```

```
// the above two statements should be placed only in the interrupt service routine invoked by the
// digital comparator. Asynchronous polling of the register will not provide a good indication of
// comparator's status
```

```
AdcRegs.ADCCOMPENA.all = ADCCOMPENA_BYTE0_COMP0_ENA +
                        ADCCOMPENA_BYTE0_COMP3_ENA +
                        ADCCOMPENA_BYTE0_COMP5_ENA;
```

```
//Means : Enable the first, the fourth and the sixth digital comparators.
```

```
AdcRegs.ADCCOMPENA.bit.COMP5_ENA = 1;
// Enable the sixth digital comparison mechanism
```

```
AdcRegs.ADCCTRL1.bit.COMP_INT_ENA = 1;
// Means: Enable Digital comparator interrupt at Local level
```

```
AdcRegs.ADCCOMPLIM5.bit.LOWER_LIMIT = 0x0FA;
// Sets the lower limit to be compared to the sixth result register
//( Note: bit does not necessarily mean one bit, but a bits field of any length
```

```
CimRegs.REQMASK.bit.REQMASK11 = 1;
// Means: Enable Digital comparator interrupt at CPU(CIM) level.
```

ADC Registers

For additional details on the UCD3000 ADC module, refer to the UCD3000 ADC Wrapper Specification document.

ADC Control Register 1 (ADCCTRL1)

Address FFF7DC00

Bit Number	22	21	20:16	15:13
Bit Name	COMP_INT_FLG	INT_FLG	CURRENT_CH	RESERVED
Access	R	R	R	-
Default	-	-	-	000

Bit Number	12	11	10	9
Bit Name	COMP_INT_ENA	INT_ENA	EXT_TRIG_ENA	SW_START
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	8	7:4	3:1	0
Bit Name	SINGLE_SWEEP	MAX_CONV	EXT_TRIG_SEL	ADC_ENA
Access	R/W	R/W	R/W	R/W
Default	0	0000	000	0

Bit 22: COMP_INT_FLG – Digital Compare Interrupt flag, read of this register clears the interrupt

0 = No Digital Compare has fired.

1 = Digital Compare has fired.

Bit 21: INT_FLG – End-of-conversion interrupt flag, read of this register clears the interrupt

0 = No End-of-conversion interrupt detected

1 = End-of-conversion interrupt found

Bits 20-16: CURRENT_CH – Register shows the currently converting channel

Bits 15-13: RESERVED – Unused bits – Default to 000

Bit 12: COMP_INT_ENA – Digital Compare Interrupt Enable

0 = Disable Digital Compare Interrupt (Default)

1 = Enable Digital Compare Interrupt

Bit 11: INT_ENA – End-of-conversion Interrupt Enable

0 = Disable End-of-Conversion Interrupt (Default)

1 = Enable End-of-Conversion Interrupt

Bit 10: EXT_TRIG_ENA – External Trigger Enable, conversions are started using the external trigger as selectable by the **EXT_TRIG_SEL** bits.

0 = Disable External Trigger capability (Default)

1 = Enable External Trigger capability

Bit 9: SW_START – Software Conversion Start

0 = Conversions not initiated by software (Default)

1 = Initiate a conversion loop

Bit 8: SINGLE_SWEEP – ADC Conversion Mode

0 = Continuous conversion loop runs (Default)

1 = Single conversion loop run

Bits 7-4: MAX_CONV – Maximum number of conversion done in one conversion loop

0x0 = 1 conversion selection converted in the loop (Default)

0xF = All 16 conversion selections converted in the loop

Bits 3-1: EXT_TRIG_SEL – Selects which external trigger can start a conversion loop.

0x0 = HS Loop1 Event 1 (DPWMA Low Resolution Edge) (Default)

0x1 = HS Loop1 Event 3 (DPWMB Low Resolution Edge)

0x2 = HS Loop2 Event 1 (DPWMA Low Resolution Edge)
 0x3 = HS Loop2 Event 3 (DPWMB Low Resolution Edge)
 0x4 = HS Loop3 Event 1 (DPWMA Low Resolution Edge)
 0x5 = HS Loop3 Event 3 (DPWMB Low Resolution Edge)
 0x6 = HS Loop4 Event 1 (DPWMA Low Resolution Edge)
 0x7 = HS Loop4 Event 3 (DPWMB Low Resolution Edge)

Bit 0: ADC_ENA – ADC12 Enable Control

0 = Disables ADC (Default)

1 = Enables ADC

ADC Test Control Register (ADCTSTCTRL)

Address FFF7DC04

Bit Number	14	13:12	11:0
Bit Name	TEMP_SENS_DIS	REF_SEL	RESERVED
Access	R/W	R/W	R/WR/W
Default	0	0	0

Bit 14: TEMP_SENS_DIS – Temperature Sensor Disable

0 = Enables Temperature Sensor (Default)

1 = Disables Temperature Sensor

Bits 13-12: ADC_SEL_REF – ADC Voltage Reference Select

00 = Selects Internal ADC voltage reference (Default)

01 = Selects AVDD as ADC voltage reference

10 = Selects External ADC voltage reference

11 = Undefined

ADC Sequence Select Register 1 (ADCSEQSEL1)

Address FFF7DC08

Bit Number	14:10	9:5	4:0
Bit Name	SEQ2	SEQ1	SEQ0
Access	R/W	R/W	R/W
Default	00000	00000	00000

Bits 14-10: SEQ2 - Channel to be converted third

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

Bits 9-5: SEQ1 - Channel to be converted second

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

Bits 4-0: SEQ0 - Channel to be converted first

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

ADC Sequence Select Register 2 (ADCSEQSEL2)

Address FFF7DC0C

Bit Number	14:10	9:5	4:0
Bit Name	SEQ5	SEQ4	SEQ3
Access	R/W	R/W	R/W
Default	00000	00000	00000

Bits 14-10: SEQ5 - Channel to be converted sixth

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

Bits 9-5: SEQ4 - Channel to be converted fifth

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

Bits 4-0: SEQ3 - Channel to be converted fourth

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

ADC Sequence Select Register 3 (ADCSEQSEL3)

Address FFF7DC10

Bit Number	14:10	9:5	4:0
Bit Name	SEQ8	SEQ7	SEQ6
Access	R/W	R/W	R/W
Default	00000	00000	00000

Bits 14-10: SEQ8 - Channel to be converted ninth

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

Bits 9-5: SEQ7 - Channel to be converted eighth

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

Bits 4-0: SEQ6 - Channel to be converted seventh

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

ADC Sequence Select Register 4 (ADCSEQSEL4)

Address FFF7DC14

Bit Number	14:10	9:5	4:0
Bit Name	SEQ11	SEQ10	SEQ9
Access	R/W	R/W	R/W
Default	00000	00000	00000

Bits 14-10: SEQ11 - Channel to be converted twelfth

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

Bits 9-5: SEQ10 - Channel to be converted eleventh

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

Bits 4-0: SEQ9 - Channel to be converted tenth

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

ADC Sequence Select Register 5 (ADCSEQSEL5)

Address FFF7DC18

Bit Number	14:10	9:5	4:0
Bit Name	SEQ14	SEQ13	SEQ12
Access	R/W	R/W	R/W
Default	00000	00000	00000

Bits 14-10: SEQ14 - Channel to be converted fifteenth

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

Bits 9-5: SEQ13 - Channel to be converted fourteenth

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

Bits 4-0: SEQ12 - Channel to be converted thirteenth

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

ADC Sequence Select Register 6 (ADCSEQSEL6)

Address FFF7DC1C

Bit Number	4:0
Bit Name	SEQ15
Access	R/W
Default	00000

Bits 4-0: SEQ15 – Channel to be converted sixteenth

00000 = Channel 0 selected (Default)

00001 = Channel 1 selected

.....

11111 = Channel 31 selected

ADC Result Registers 0-15 (ADCRESULT_x, x=0:15)

Address FFF7DC20 – ADC Result Register 0

Address FFF7DC24 – ADC Result Register 1

Address FFF7DC28 – ADC Result Register 2

Address FFF7DC2C – ADC Result Register 3

Address FFF7DC30 – ADC Result Register 4

Address FFF7DC34 – ADC Result Register 5

Address FFF7DC38 – ADC Result Register 6

Address FFF7DC3C – ADC Result Register 7

Address FFF7DC40 – ADC Result Register 8

Address FFF7DC44 – ADC Result Register 9

Address FFF7DC48 – ADC Result Register 10

Address FFF7DC4C – ADC Result Register 11

Address FFF7DC50 – ADC Result Register 12

Address FFF7DC54 – ADC Result Register 13

Address FFF7DC58 – ADC Result Register 14

Address FFF7DC5C – ADC Result Register 15

Bit Number	11:0
Bit Name	RESULT
Access	R
Default	-

Bits 11-0: RESULT – Each sequence has a dedicated result register.

ADC Digital Compare Limits Register 0-5 (ADCCOMPLIMx, x=0:5)

Address FFF7DC60 – ADC Digital Compare Limits Register 0

Address FFF7DC64 – ADC Digital Compare Limits Register 1

Address FFF7DC68 – ADC Digital Compare Limits Register 2

Address FFF7DC6C – ADC Digital Compare Limits Register 3

Address FFF7DC70 – ADC Digital Compare Limits Register 4

Address FFF7DC74 – ADC Digital Compare Limits Register 5

Bit Number	27:16	15:12	11:0
Bit Name	UPPER_LIMIT	RESERVED	LOWER_LIMIT
Access	R/W	-	R/W
Default	1111_1111_1111	0000	0000_0000_0000

Bits 27-16: UPPER_LIMIT – Configures the upper limit value. If the ADC conversion selected is equal or greater than the limit, the Digital Compare Interrupt Flag is set (bit 22 of ADC Control Register 1). Results of comparison can be read from the ADC Digital Compare Results Register (see Section 4.12).

Bits 15-12: RESERVED – Unused bits – Default to 0000

Bits 11-0: LOWER_LIMIT – Configures the lower limit value. If the ADC conversion selected is equal or less than the limit, the Digital Compare Interrupt Flag is set (bit 22 of ADC Control Register 1). Results of comparison can be read from the ADC Digital Compare Results Register (see Section 4.12).

ADC Digital Compare Enable Register (ADCCOMPENA)

Address FFF7DC78

Bit Number	5	4	3
Bit Name	COMP5_ENA	COMP4_ENA	COMP3_ENA
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	COMP2_ENA	COMP1_ENA	COMP0_ENA
Access	R/W	R/W	R/W
Default	0	0	0

Bit 5: COMP5_ENA – Digital Comparator 5 Enable

0 = Digital Comparator 5 Disabled (Default)

1 = Digital Comparator 5 Enabled

Bit 4: COMP4_ENA – Digital Comparator 4 Enable

0 = Digital Comparator 4 Disabled (Default)

1 = Digital Comparator 4 Enabled

Bit 3: COMP3_ENA – Digital Comparator 3 Enable

0 = Digital Comparator 3 Disabled (Default)

1 = Digital Comparator 3 Enabled

Bit 2: COMP2_ENA – Digital Comparator 2 Enable

0 = Digital Comparator 2 Disabled (Default)

1 = Digital Comparator 2 Enabled

Bit 1: COMP1_ENA – Digital Comparator 1 Enable

0 = Digital Comparator 1 Disabled (Default)

1 = Digital Comparator 1 Enabled

Bit 0: COMP0_ENA – Digital Comparator 0 Enable

0 = Digital Comparator 0 Disabled (Default)

1 = Digital Comparator 0 Enabled

ADC Digital Compare Results Register (ADCCOMPRESULT)

Address FFF7DC7C

Bit Number	11:10	9:8	7:6
Bit Name	RESULT5	RESULT4	RESULT3
Access	R	R	R
Default	-	-	-

Bit Number	5:4	3:2	1:0
Bit Name	RESULT2	RESULT1	RESULT0
Access	R	R	R
Default	-	-	-

Bits 11-10: RESULT5 – Digital Comparator 5 Result

Bit 11: Upper Limit Indication

0 = Limit not exceeded

1 = Limit exceeded

Bit 10: Lower Limit Indication

0 = Limit not exceeded

1 = Limit exceeded

Bits 9-8: RESULT4 – Digital Comparator 4 Result

Bit 9: Upper Limit Indication

0 = Limit not exceeded

1 = Limit exceeded

Bit 8: Lower Limit Indication

0 = Limit not exceeded

1 = Limit exceeded

Bits 7-6: RESULT3 – Digital Comparator 3 Result

Bit 7: Upper Limit Indication

0 = Limit not exceeded

1 = Limit exceeded

Bit 6: Lower Limit Indication

0 = Limit not exceeded

1 = Limit exceeded

Bits 5-4: RESULT2 – Digital Comparator 2 Result

Bit 5: Upper Limit Indication

0 = Limit not exceeded

1 = Limit exceeded

Bit 4: Lower Limit Indication

0 = Limit not exceeded

1 = Limit exceeded

Bits 3-2: RESULT1 – Digital Comparator 1 Result

Bit 3: Upper Limit Indication

0 = Limit not exceeded

1 = Limit exceeded

Bit 2: Lower Limit Indication

0 = Limit not exceeded

1 = Limit exceeded

Bits 1-0: RESULT0 – Digital Comparator 0 Result

Bit 1: Upper Limit Indication

0 = Limit not exceeded

1 = Limit exceeded

Bit 0: Lower Limit Indication

0 = Limit not exceeded

1 = Limit exceeded